



LED Driving

Sizing

We expect 16 RGB LED rings encoders. So let's do the math : **16 Encoders * 32 LEDs * 3 colors = 1536 lines**

Let's transpose this to a classical matrixed SRIO chain design:

16 * 3 (cathodes) * 32 (anodes)
= 48 inputs + 32 outputs
= 6*DIN + 4*DOUT

Core-External Driving Concept : TLC5958

In theory it's possible to drive such a SRIO setup but in fact buses and resistors/R networks are very hard to place and it will consume a lot of constant refresh process.

After a look on the different brands and models of LED driver IC **Texas Instruments TLC5958** appeared as a good compromise to drive a lot of RGB LEDs without overloading the core. Designed to be a LED Display driver, its original purpose and features would allow large-sized RGB-LED-based display setups

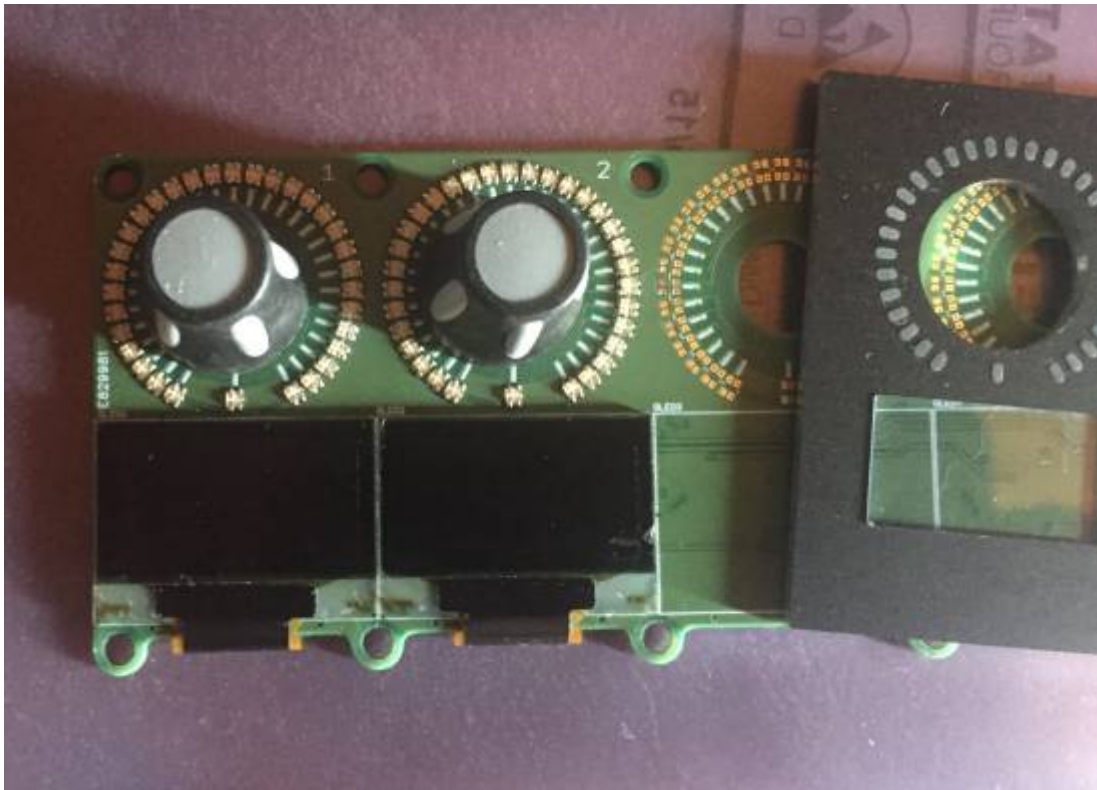
[TLC5958 Datasheet](#)

This Design note from Texas Instruments helps in understanding how to design around the TLC:
[Build high density, high refresh rate, multiplexing LED panel with TLC5958](#)

TLC5958 Features

1. **48 Channels Constant Current Sink Output**

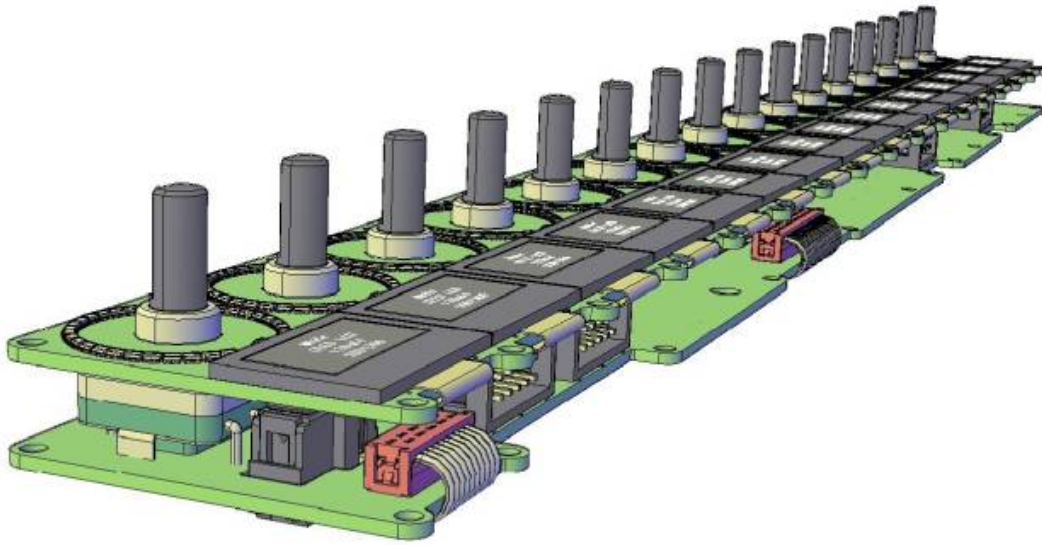
Distance between SMD LEDs center is somewhat close (2.0046mm) But not impossible, for proof:



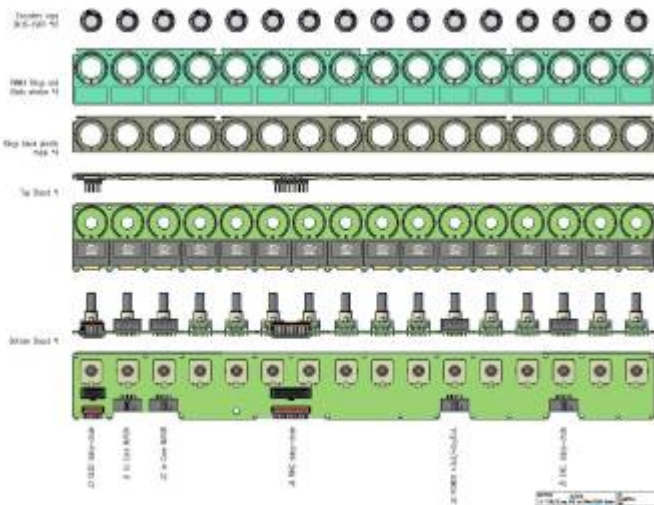
Conceptual views

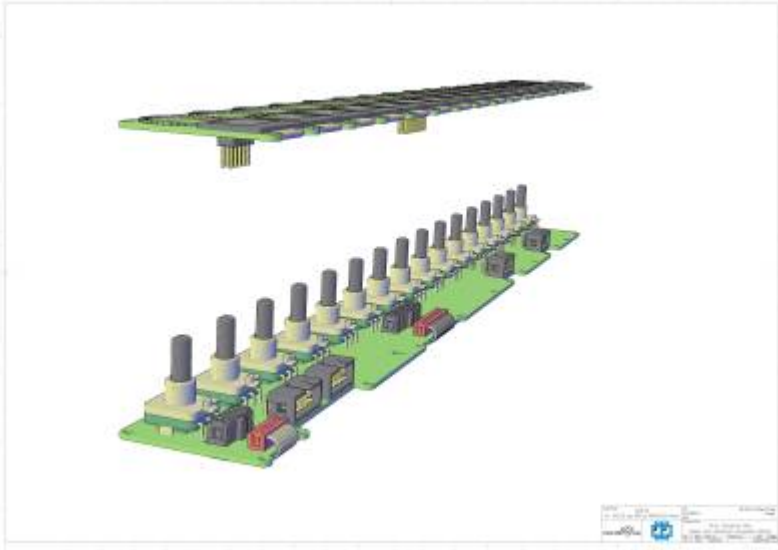
The module consists in a 2 pcbs sandwich, spaced 10mm .

Global size is 432mm Width * 50mm Height * 22mm Depth



ProjName	OLRE16	Rev	00000000000000000000
Proj #	OLRE16	Rev #	00000000000000000000
Proj Path	OLRE16	Rev Path	OLRE16
Proj Desc	OLRE16	Rev Desc	OLRE16
Proj Author	OLRE16	Rev Author	OLRE16
Proj Date	OLRE16	Rev Date	OLRE16
Proj Status	OLRE16	Rev Status	OLRE16
Proj Category	OLRE16	Rev Category	OLRE16
Proj Subcategory	OLRE16	Rev Subcategory	OLRE16
Proj Description	OLRE16	Rev Description	OLRE16
Proj Notes	OLRE16	Rev Notes	OLRE16
Proj Comments	OLRE16	Rev Comments	OLRE16
Proj History	OLRE16	Rev History	OLRE16
Proj Changes	OLRE16	Rev Changes	OLRE16
Proj Issues	OLRE16	Rev Issues	OLRE16
Proj Risks	OLRE16	Rev Risks	OLRE16
Proj Dependencies	OLRE16	Rev Dependencies	OLRE16
Proj Constraints	OLRE16	Rev Constraints	OLRE16
Proj Assumptions	OLRE16	Rev Assumptions	OLRE16
Proj Risks	OLRE16	Rev Risks	OLRE16
Proj Dependencies	OLRE16	Rev Dependencies	OLRE16
Proj Constraints	OLRE16	Rev Constraints	OLRE16
Proj Assumptions	OLRE16	Rev Assumptions	OLRE16







Prototyping

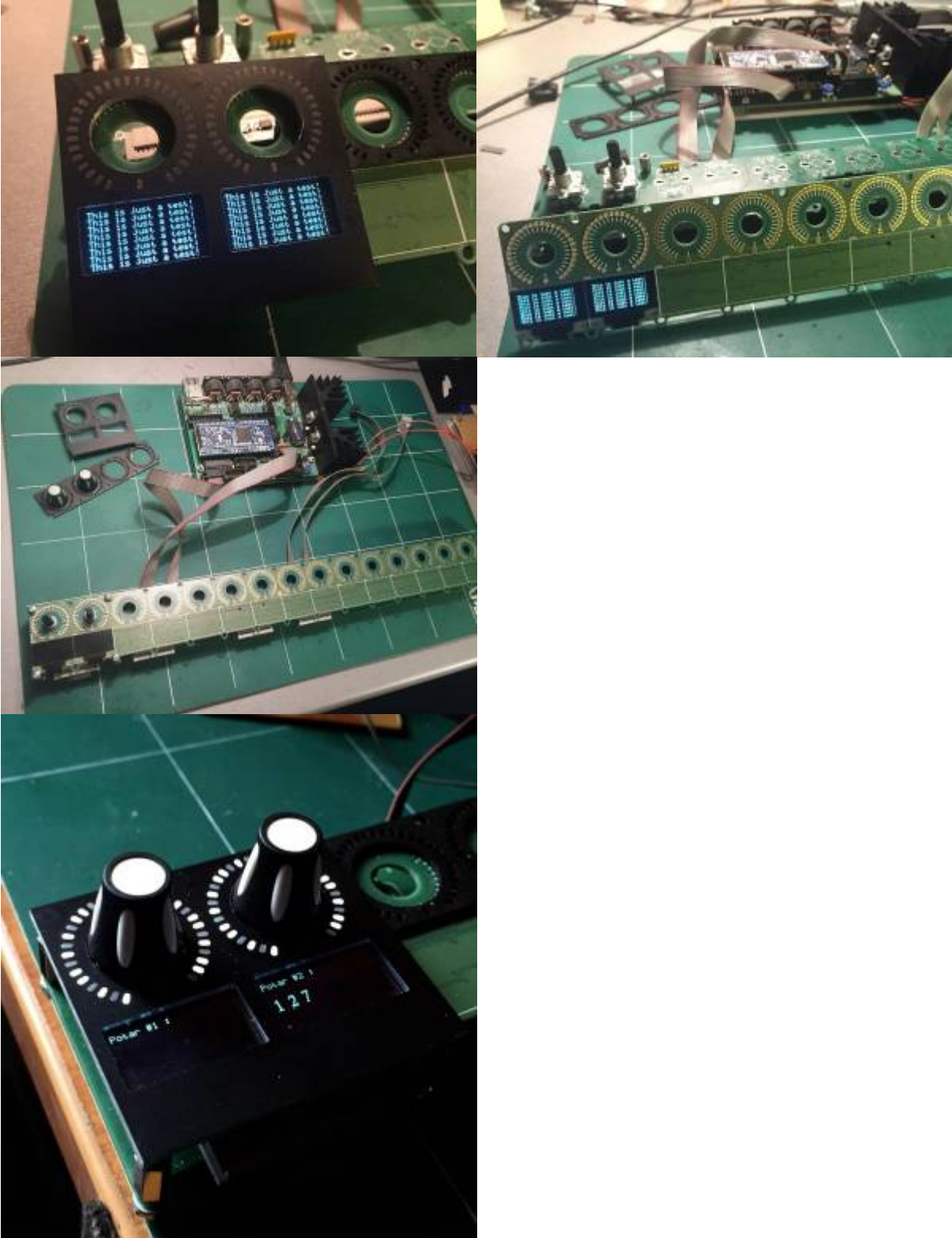
The first prototype was tested with an [LPC1769 Core](#). For testing purposes only 2 LED-rings were set up in order not to waste components for development. The first software module written was added in an app, but integration in the SEQ V4 app was not possible because a lack of Memory on the LPC17 Core...

Meanwhile the migration to [STM32F4 Core](#), an independent external clocking circuit for the GSCLK and the address lines was designed. STM32F4 Core will just have to provide a PWM a RESET signal and receive an interrupt from this circuit to get the End Of Frame.

Data Transfer

A serialized design has been chosen to provide data to TLC. Prototype feature only 2 steps but the CORE works like there's 4 modules of 16 steps connected. In order to benchmark reactivity and Transfer time, Core send data for 4 modules ($4 \times 16 \times 32 \times 3 \times 16 \text{bit} = 12 \text{KBytes}$). Through an emulated software SPI bus, for this 64 rings Data Sending takes less than 5ms . Different colors and patterns

like relative value(-64/63), keyboard(B&W keys) etc... were tested.





GrayScale Clock

Design of External GrayScale Clock for the TLC was tricky.

257 clock periods and halt for some 1.5~2.5 μ s are needed for each address line

TLC would receive a VSYNC command at the end of the 32th address line to prepare the new frame datas.

The first approach was to provide a PWM at 800KHz and put it back to the LPC on a TMR CAP Input, use 2 MAT outputs to provide a line period and gate(NOR) the PWM with it.

*First issue, halting time after the 257 periods wasn't constant and dependent of PWM frequency.
Second issue, much I/O used only for this purpose.*

Electronic Design

TLC related Design



Figure 1. Typical Application Circuit (Multiple Daisy Chained TLC5958s)

Example: 8+8 mode, Multiplexing ratio 1/32



Figure 16. Controller Timing Sequence, 8+8 Mode, 32 Multiplexing

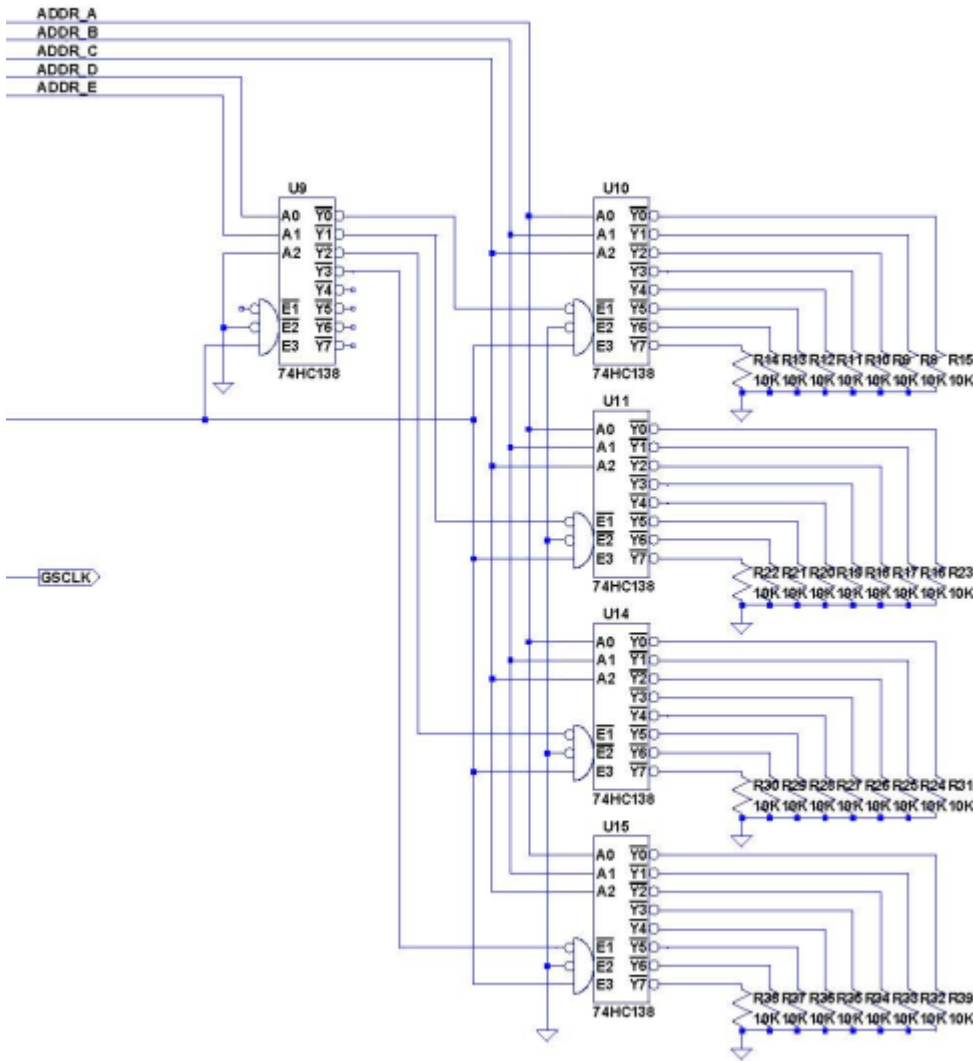
TLC is wired like on an SPI bus to Core Board. Here are connections equivalences:

- SCLK ⇒ SC
- DATA ⇒ SO
- LAT ⇒ RC

After a certain time given by the RC couple on U1, U1 switch back and restarts the counter. By this way we are sure to count the exact 257 Clocks needed and the interval between 2 segments is fixed by the trimpot U19.

GSCLK signal is then high during the 257 clocks period and low during the interval

Multiplexing Schematic



ADDR_x, ADDR_CLK, GSCLK are connected to the top board...

ADDR_CLK is the multiplexed lines clock . It's used to gate the PWM signal and obtain the GSCLK and of course, as a clock for the ADDR Counter U5. The counter U5 provides the coded ADDR_x lines and an EOF(End Of Frame) when 32 is reached.

To be continued... 😊

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